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Table of Contents

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Note : Remove "Table of Content" before including in CP Book

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

17EC53 : Verilog HDL

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	UG
Year / Semester :	3/5	Academic Year:	2019-20
Course Title:	VERILOG HDL	Course Code:	17EC53
Credit / L-T-P:	4/4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50	SEE Marks:	80 Marks
CIA Marks:	20	Assignment	1 / Module
Course Plan Author:	NARASIMHA MURTHY R	Sign	Dt:
Checked By:	Dr. DEVANANDA S N	Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	**Overview of Digital Design with Verilog HDL** Evolution of CAD, emergence of HDLs, typical HDL-flow, why Verilog HDL?, trends in HDLs. **Hierarchical Modeling Concepts** Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block,stimulus block.	10	Fundamental of HDL Design methodologies	L2,L3
2	**Basic Concepts** Lexical conventions, data types, system tasks, compiler directives. **Modules and Ports** Module definition, port declaration, connecting ports, hierarchical name referencing	10	Basics of verilog programming and syntax	L2,L3
3	**Gate-Level Modeling** Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off	14	Verilog programming	L2,L3

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	delays, min, max, and typical delays **Data-flow Modeling** Continuous assignments, delay specification, expressions, operators, operands, operator types..		at Gate-level and data flow level	
4	**Behavioral Modeling** Structured procedures, initial and always, blocking and non-blocking statements. delay control, generate statement, event control, conditional statements, Multi-way branching, loops, sequential and parallel blocks.	12	Verilog programming at behaviourallevel modeling	L2,L3
5	**Introduction to VHDL** Introduction: Why use VHDL?, Shortcomings, Using VHDL for Design Synthesis, Design tool flow, Font conventions. **Entities and Architectures:** Introduction, A simple design, Design entities, Identifiers, Data objects, Data types, and Attributes	12	VHDL Programming	L2,L3

3. Course Material

Module	Details	Available
1	Text books	
	Samir Palnitkar, “ Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education, Second Edition.	In Lib
	Kevin Skahill, “VHDL for Programmable Logic”, PHI/Pearson education, 2006	
2	Reference books	
	Donald E. Thomas, Philip R. Moorby, “The Verilog Hardware Description Language”, Springer Science+Business Media, LLC, Fifth edition.	In dept
	Michael D. Ciletti, “Advanced Digital Design with the Verilog HDL” Pearson (Prentice Hall), Second edition.	
	Padmanabhan, Tripura Sundari, “Design through Verilog HDL”, Wiley, 2016	
3	Others (Web, Video, Simulation, Notes etc.)	
	• https://www.youtube.com/watch?v=BI_2p9E6kXE • https://www.youtube.com/watch?v=z2ivjyBiTG8 • https://www.youtube.com/watch?v=6g57UkQKpKA	Available
	• https://www.youtube.com/watch?v=CUgIisaMbS4 • https://www.youtube.com/watch?v=CsnZ9K0fPl8	

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	• https://www.youtube.com/watch?v=39SvQ55e7po • https://www.youtube.com/watch?v=uLqIHN-0Kao	
	• https://www.youtube.com/watch?v=3yRPvy4ILEw • https://www.youtube.com/watch?v=1MSDwnLEHks • https://www.youtube.com/watch?v=VUEFqHdh0L0 • https://www.youtube.com/watch?v=IX4aK7Buv_Y	
	• https://www.youtube.com/watch?v=9YQss26VcBw • https://www.youtube.com/watch?v=uSLJ0UQvzfQ • https://www.youtube.com/watch?v=zwg2fIo3sJQ • https://www.youtube.com/watch?v=TKMFpg3yKT0 • https://www.youtube.com/watch?v=VBUyqOyeueI • https://www.youtube.com/watch?v=xmeAM0BfNck • https://www.youtube.com/watch?v=fPIJTh1ZfYU	

4. Course Prerequisites

SNo	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	17ELN25	Basic electronics	3/Digital electronics/ Knowledge on Basic gates	1		L2
2	17EC33	Digital electronics	2/Analysis and design of combinational logic/Knowledge of Combinational and sequential logic circuits	3		L2,L3, L4
3	17EC33	Digital electronics	3/Flip-flops/Knowledge of Combinational and sequential logic circuits	3		L2,L3, L4

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
17EC53.1	Understanding the need of HDLs and CAD tools in digital system design.	05	Hardware Description Language	Lecture	Slip Test	L2 Understand
17EC53.2	Acquiring the knowledge on hierarchical design methodologies	05	Design methodology	Lecture	Slip Test	L2 Understand

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	to solve digital system design problems					
17EC53.3	Analyzing the structure of verilog program.	10	Verilog programming syntax	Lecture	Assignment and Slip Test	L3 Apply
17EC53.4	Understand Verilog Tasks and Directives.		Tasks and Directives.	Lecture	Assignment and Slip Test	L2 Understand
17EC53.5	Design digital circuits using gate level modeling with test bench	06	Verilog programming at gate level	Lecture and Tutorial	Assignment and Slip Test	L3 Apply
17EC53.6	Design digital circuits using data-flow level modeling with test bench	06	Verilog programming at data-flow level	Lecture and Tutorial	Assignment and Slip tes	L3 Apply
17EC53.7	Design digital circuits using behavioral style of modeling with test bench	07	Verilog programming in behavioral level	Lecture and Tutorial	Assignment and Slip test	L3 Apply
17EC53.8	Acquiring the knowledge on basics of VHDL and difference between verilog and VHDL	07	VHDL Fundamentals	Lecture and Tutorial	Assignment and Slip Test	L2 Understand
17EC53.9	Design digital circuits using VHDL programming.	06	VHDL Programming	Lecture	Assignment	L3 Apply
-	**Total**	**58**	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	Understanding the design of digital system	CO1	L2
2	Understanding verilog programming techniques	CO2	L2
3	Apply Verilog programming at gate level in design of System on Chip	CO3	L3
4	Apply Verilog programming at data flow level in design of ASIC	CO4	L3
5	Apply Verilog programming at behavioral level in design of microprocessors	CO5	L3
6	Apply Verilog programming at behavioral level in design of microcontrollers	CO6	L3
7	Understanding VHDL programming techniques	CO7	L2
8	Apply VHDL programming in the design of digital circuits	CO8	L3

Note: Write 1 or 2 applications per CO.

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3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes											
#	COs	PO 1	PO2	PO 3	PO 4	PO 5	PO6	PO 7	PO 8	PO9	PO 10	PO 11	PO 12	Level
17EC53.1	Understanding the need of HDLs and CAD tools in digital system design.	3	3	3	3	3				2				L2
17EC53.2	Acquiring the knowledge on hierarchical design methodologies to solve digital system design problems	3	3	3		3				2				L3
17EC53.3	Analyzing the structure of verilog program.	3	3			3				2				L3
17EC53.4	Understand Verilog Tasks and Directives.	3				3				2				L2
17EC53.5	Design digital circuits using gate level modeling with test bench	2	3	3	3	3				2				L3
17EC53.6	Design digital circuits using data-flow level modeling with test bench	2	3	3	3	3				2				L3
17EC53.7	Design digital circuits using behavioral style of modeling with test bench	2	3	3	3	3				2				L3
17EC53.8	Acquiring the knowledge on basics of VHDL and difference between verilog and VHDL	2				3				1				L2
17EC53.9	Design digital circuits using VHDL programming.	2	3	3	3	3				2				L3
Note: Mention the mapping strength as 1, 2, or 3														

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**	**-**	**-**
CO1	PO1	Knowledge of basic HDL is required to build any digital system systems	L1
CO1	PO2	Analysis and getting solution of hardware extractions for reduced complexity requires knowledge of HDL.	L3

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CO1	PO3	Design and development is required.	L3
CO1	PO5	Tool is available for simulation.	L3
CO1	PO9	Involves lab experiments, mini projects, projects and internships.	L3
CO2	PO1	Knowledge of hierarchical design methodologies is required in building complex digital systems.	L1
CO2	PO2	Optimizing the complex problems for efficient implementation requires knowledge of modularity.	L3
CO2	PO3	Design and computing of digital system that meet specific needs.	L3
CO2	PO4	Digital system design methodologies required for snslyding the complex digital systems.	L3
CO2	PO5	Tool exists for design and implementation.	L3
CO2	PO9	Digital system design knowledge is required to carryout projects and internships in VLSI domain.	L3
CO3	PO1	Verilog programming syntax is required in building digital system design.	L3
CO3	PO2	Compact and efficient system implementation.	L3
CO3	PO5	Tool exists for verilog design.	L3
CO3	PO9	Structure of programming syntax needed for lab experiments.	L3
CO4	PO1	Knowledge of tasks and directives are required for solutions of complex engineering problems.	L1
CO4	PO5	Existing tools uses the directives for providing results.	L3
CO4	PO9	Directives and tasks are used for every lab programs.	L3
CO5	PO1	Required to build solutions of complex engineering problems.	L3
CO5	PO2	Analysis of digital systems working requires the simulation and hardware implementation.	L3
CO5	PO3	Complex engineering systems start with gate level designing.	L3
CO5	PO4	Tool exists for gate level design.	L3
CO5	PO9	Gate level modeling is the one way to design digital systems in projects and lab experiments.	L3
CO6	PO1	Required to build solutions of complex engineering problems.	L3
CO6	PO2	Analysis of digital systems working requires the simulation and hardware implementation.	L3
CO6	PO3	Complex engineering systems start with dataflow level designing.	L3
CO6	PO4	Tool exists for gate level design.	L3
CO6	PO9	dataflow level modeling is the one way to design digital systems in projects and lab experiments.	L3
CO7	PO1	Required to build solutions of complex engineering problems.	L3
CO7	PO2	Analysis of digital systems working requires the simulation and	L3

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		hardware implementation.	
CO7	PO3	Complex engineering systems start with behavioral level designing.	L3
CO7	PO4	Tool exists for gate level design.	L3
CO7	PO9	behavioral level modeling is the one way to design digital systems in projects and lab experiments.	L3
CO8	PO1	Required for solution of complex engineering problems.	L3
CO8	PO5	Modern tool exists for vhdl and verilog.	L3
CO8	PO9	All interfacing programs to be done with both verilog and vhdl.	L3
CO9	PO1	Required to build solutions of complex engineering problems.	L2
CO9	PO2	Analysis of digital systems working requires the simulation and hardware implementation.	L3
CO9	PO3	Complex engineering systems to be done vhdl.	L3
CO9	PO4	Tool exists for gate level design.	L3
CO9	PO9	VHDL is the one way to design digital systems in projects and lab experiments.	L3

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					

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9					
10					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Module #	Title	Teaching Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Overview of Digital Design with Verilog HDL and Hierarchical Modeling Concepts	10	2	-	-	1	1	2	CO1, CO2	L2, L3
2	Basic Concepts and Modules and Ports	10	2	-	-	1	1	2	CO3, CO4	L3 L3
3	Gate Level Modeling and Data flow Modeling	12	-	2	-	1	1	2	CO5, CO6	L3, L3
4	Behavioral Modeling	14	-	2	-	1	1	2	C07	L23 L3
5	Introduction to VHDL and	12	-	-	4	1	1	2	CO8, CO9	L2, L3
-	**Total**	**58**	**4**	**4**	**4**	**5**	**5**	**10**	**-**	**-**

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	15	CO1, CO2,CO3, CO4	L2, L3,
CIA Exam – 2	15	CO5,CO6,CO7	L2, L3,
CIA Exam – 3	15	CO8,CO9	L2, L3,
Assignment – 1	03	CO1, CO2,CO3, CO4	L2, L3,
Assignment – 2	03	CO5,CO6,CO7	L2, L3,
Assignment – 3	03	CO8,CO9	L2, L3,
Seminar – 1	02	CO1, CO2,CO3, CO4	L2, L3, L4,
Seminar – 2	02	CO5,CO6,CO7	L2, L3, L4,
Seminar – 3	02	CO8,CO9	L2, L3, L4,

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Other Activities – define – Slip test		CO1 to CO9	L2, L3, L4
Final CIA Marks	**40**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN – 1

Module – 1

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Acquiring the knowledge on digital design and different modeling concepts	CO1	L2
2			
b	***Course Schedule***	–	–
Class No	**Module Content Covered**	**CO**	**Level**
1	**Overview of Digital Design with Verilog HDL** Evolution of CAD	C01	L2
2	Emergence of HDLs	C01	L2
3	Typical HDL-flow, why Verilog HDL?	C01	L2
4	Trends in HDLs	C01	L2
5	**Hierarchical Modeling Concepts** Top-down design methodology,	CO2	L2
6	Bottom-up design methodology	CO2	L2
7	differences between modules and module instances	CO2	L2
8	Parts of a simulation,	CO2	L2
9	Design block	CO2	L2
10	Stimulus block	CO2	L2
c	**Application Areas**	**CO**	**Level**
1	Understanding the design of digital system	CO1, CO2	L2
2			
d	**Review Questions**	–	–
1	Discuss in brief about the evolution of CAD tools and HDLs used in digital system design	CO1	L2
2	Explain the typical VLSI IC design flow with the help of flow chart.	CO1	L2
3	Discuss the trends in HDLs?	CO1	L2

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4	Why Verilog HDL has evolved as popular HDL in digital circuit design?	CO1	L2
5	Explain the advantages of using HDLs over traditional schematic based design.	CO1	L2
6	Describe the digital system design using hierarchical design methodologies.	CO2	L2
7	Apply the top-down design methodology to demonstrate the design of ripple carry counter.	CO2	L3
8	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	CO2	L3
9	Write Verilog HDL program to describe the 4-bit ripple carry counter.	CO2	L3
10	Define Module and an Instance. Describe 4 different description styles of Verilog HDL	CO2	L2
11	Differentiate simulation and synthesis. What is stimulus?	CO2	L3
12	Write a test bench to test the 4-bit ripple carry counter.	CO2	L3
13	Write a test bench to test the 4-bit ripple carry adder.	CO2	L3
e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module - 2

Title:	Divide and Conquer	Appr Time:	10 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Analyzing the structure of verilog program and usage of tasks and directives	CO3	L4
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
1	**Basic Concepts** Lexical conventions,	CO3	L2
2	Lexical conventions,	CO3	L2
3	data types,	CO3	L2
4	data types	CO3	L2
5	system tasks,	CO3	L2
6	compiler directives.	CO3	L2

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7	**Modules and Ports** Module definition,	CO4	L3
8	port declaration,	CO4	L3
9	connecting ports,	CO4	L3
10	hierarchical name referencing	CO4	L3
c	**Application Areas**	**CO**	**Level**
1	Writing verilog programs to design digital systems.	CO3	L3
2			
d	**Review Questions**	-	-
1	Describe the lexical conventions used in Verilog HDL with examples.	CO3	L2
2	Explain different data types of Verilog HDL with examples	CO3	L2
3	What are system tasks and compiler directives?	CO3	L2
4	What are the uses of $monitor, $display and $finish system tasks? Explain with examples.	CO3	L2
5	Explain `define, `timescale and `include compiler directives.	CO3	L2
6	Explain the components of Verilog HDL module.	CO4	L2
7	What are the components of SR latch? Write Verilog HDL module of SR latch.	CO4	L3
8	Explain the different types of ports supported by Verilog HDL with examples.	CO4	L3
9	Explain the port connection rules of Verilog HDL with examples.	CO4	L3
10	How hierarchical names helps in addressing any identifier used in the design from any other level of hierarchy? Explain with examples.	CO4	L3
11	What are the basic components of a module? Which components are mandatory?	CO4	L2
e	**Experiences**	-	-
1			
2			
3			
4			
5			

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E1. CIA EXAM – 1

a. Model Question Paper – 1

Crs Code:	15EC53	Sem:	5	Marks:	30	Time:	75 minutes
Course:	Verilog HDL						

-	-	**Note: Answer any ONE questions from each module.**	**Marks**	**CO**	**Level**
		MODULE-1			
1	a	Explain the typical VLSI IC design flow with the help of flow chart.	08	CO1	L2
	b	Explain the advantages of using HDLs over traditional schematic based design	07	CO1	L2
2	a	Describe the digital system design using hierarchical design methodologies.	08	CO2	L2
	b	Define Module and an Instance. Describe 4 different description styles of Verilog HDL	07	CO2	L2
		MODULE-2			
3	a	Explain different data types of Verilog HDL with examples	08	CO3	L2
	b	What are the components of SR latch? Write Verilog HDL module of SR latch.	07	CO3	L2
4	a	Explain `define, `timescale and `include compiler directives.	08	CO4	L2
	b	Explain the components of Verilog HDL module.	07	CO4	L2

b. Assignment –1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	15EC53	Sem:	5	Marks:	3 / 5	Time:	90 – 120 minutes
Course:	Verilog HDL						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	**USN**	**Assignment Description**	**Marks**	**CO**	**Level**
1.	1KT16EC003	Discuss in brief about the evolution of CAD tools and HDLs used in digital system design	5	CO1	L2
2.	1KT16EC004	Explain the typical VLSI IC design flow with the help of flow chart.	5	CO1	L2
3.	1KT16EC005	Discuss the trends in HDLs?	5	CO1	L2
4.	1KT16EC008	Why Verilog HDL has evolved as popular HDL in digital circuit design?	5	CO1	L2

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5.	1KT16EC011	Explain the advantages of using HDLs over traditional schematic based design.	5	CO1	L2
6.	1KT16EC012	Describe the digital system design using hierarchical design methodologies.	5	CO2	L2
7.	1KT16EC014	Apply the top-down design methodology to demonstrate the design of ripple carry counter.	8	CO2	L2
8.	1KT16EC015	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	8	CO2	L2
9.	1KT16EC016	Write Verilog HDL program to describe the 4-bit ripple carry counter.	8	CO2	L2
10.	1KT16EC018	Define Module and an Instance. Describe 4 different description styles of Verilog HDL	8	CO2	L2
11.	1KT16EC020	Differentiate simulation and synthesis. What is stimulus?	8	CO2	L2
12.	1KT16EC022	Write a test bench to test the 4-bit ripple carry counter.	8	CO2	L3
13.	1KT16EC023	Write a test bench to test the 4-bit ripple carry adder.	8	CO2	L3
14.	1KT16EC024	Describe the lexical conventions used in Verilog HDL with examples.	8	CO3	L2
15.	1KT16EC025	Explain different data types of Verilog HDL with examples	8	CO3	L2
16.	1KT16EC026	What are system tasks and compiler directives?	8	CO3	L2
17.	1KT16EC027	What are the uses of $monitor, $display and $finish system tasks? Explain with examples.	8	CO3	L2
18.	1KT16EC028	Explain `define, `timescale and `include compiler directives.	8	CO3	L2
19.	1KT16EC029	Explain the components of Verilog HDL module.	8	CO3	L2
20.	1KT16EC032	What are the components of SR latch? Write Verilog HDL module of SR latch.	8	CO3	L3
21.	1KT16EC033	Explain the different types of ports supported by Verilog HDL with examples.	8	CO3	L2
22.	1KT16EC035	Explain the port connection rules of Verilog HDL with examples.	8	CO4	L2
23.	1KT16EC407	How hierarchical names helps in addressing any identifier used in the design from any other level of hierarchy? Explain with examples.	8	CO4	L2
24.	1KT16EC410	What are the basic components of a module? Which components are mandatory?	8	CO4	L2
25.	1KT16EC41	Discuss in brief about the evolution of CAD tools and	5	CO1	L2

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	3	HDLs used in digital system design			
26.	1KT16EC417	Explain the typical VLSI IC design flow with the help of flow chart.	5	CO1	L2
27.	1KT16EC425	Discuss the trends in HDLs?	5	CO1	L2
28.	1KT15EC016	Why Verilog HDL has evolved as popular HDL in digital circuit design?	5	CO1	L2
29.	1KT15EC027	Explain the advantages of using HDLs over traditional schematic based design.	5	CO1	L2
30.	1KT15EC066	Describe the digital system design using hierarchical design methodologies.	5	CO2	L2
31.	1KT16EC041	Apply the top-down design methodology to demonstrate the design of ripple carry counter.	8	CO2	L2
32.	1KT16EC042	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	8	CO2	L2
33.	1KT16EC043	Write Verilog HDL program to describe the 4-bit ripple carry counter.	8	CO2	L2
34.	1KT16EC044	Define Module and an Instance. Describe 4 different description styles of Verilog HDL	8	CO2	L2
35.	1KT16EC045	Differentiate simulation and synthesis. What is stimulus?	8	CO2	L2
36.	1KT16EC047	Write a test bench to test the 4-bit ripple carry counter.	8	CO2	L3
37.	1KT16EC048	Write a test bench to test the 4-bit ripple carry adder.	8	CO2	L3
38.	1KT16EC049	Describe the lexical conventions used in Verilog HDL with examples.	8	CO3	L2
39.	1KT16EC050	Explain different data types of Verilog HDL with examples	8	CO3	L2
40.	1KT16EC051	What are system tasks and compiler directives?	8	CO3	L2
41.	1KT16EC052	What are the uses of $monitor, $display and $finish system tasks? Explain with examples.	8	CO3	L2
42.	1KT16EC053	Explain `define, `timescale and `include compiler directives.	8	CO3	L2
43.	1KT16EC057	Explain the components of Verilog HDL module.	8	CO3	L2
44.	1KT16EC058	What are the components of SR latch? Write Verilog HDL module of SR latch.	8	CO3	L3
45.	1KT16EC059	Explain the different types of ports supported by Verilog HDL with examples.	8	CO3	L2
46.	1KT16EC06	Explain the port connection rules of Verilog HDL with	8	CO4	L2

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	1	examples.			
47.	1KT16EC063	How hierarchical names helps in addressing any identifier used in the design from any other level of hierarchy? Explain with examples.	8	CO4	L2
48.	1KT16EC064	What are the basic components of a module? Which components are mandatory?	8	CO4	L2
49.	1KT16EC066	Apply the top-down design methodology to demonstrate the design of ripple carry counter.	8	CO2	L2
50.	1KT16EC067	Apply the bottom-up design methodology to demonstrate the design of 4-bit ripple carry adder.	8	CO2	L2
51.	1KT16EC068	Write Verilog HDL program to describe the 4-bit ripple carry counter.	8	CO2	L2
52.	1KT16EC069	Define Module and an Instance. Describe 4 different description styles of Verilog HDL	8	CO2	L2
53.	1KT16EC070	Differentiate simulation and synthesis. What is stimulus?	8	CO2	L2
54.	1KT16EC073	Write a test bench to test the 4-bit ripple carry counter.	8	CO2	L3
55.	1KT16EC074	Write a test bench to test the 4-bit ripple carry adder.	8	CO2	L3
56.	1KT16EC077	Describe the lexical conventions used in Verilog HDL with examples.	8	CO3	L2
57.	1KT16EC078	Explain different data types of Verilog HDL with examples	8	CO3	L2
58.	1KT17EC402	What are system tasks and compiler directives?	8	CO3	L2
59.	1KT17EC403	What are the uses of $monitor, $display and $finish system tasks? Explain with examples.	8	CO3	L2
60.	1KT17EC406	Write a test bench to test the 4-bit ripple carry counter.	8	CO3	L2
61.	1KT17EC408	Write a test bench to test the 4-bit ripple carry adder.	8	CO3	L2
62.	1KT16EC079	Describe the lexical conventions used in Verilog HDL with examples.	8	CO3	L2
63.	1KT16EC080	Explain different data types of Verilog HDL with examples	8	CO3	L2

D2. TEACHING PLAN - 2

Module - 3

Title:	Divide and Conquer	Appr	16 Hrs

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		Time:	
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Design digital circuits using gate level modeling with test bench	CO5	L3
2	Design digital circuits using data-flow level modeling with test bench	CO6	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	**Gate-Level Modeling** Modeling using basic Verilog gate primitives	CO5	L3
2	Description Of And/Or And Buf/Not Type Gates	CO5	L3
3	Description Of Buf/Not Type Gates	CO5	L3
4	Rise, Fall And Turn-Off Delays	CO5	L3
5	Min, Max, And Typical Delays	CO6	L2
6	**Data-flow Modeling** Continuous assignments,	CO6	L3
7	Delay Specification	CO6	L3
8	Expressions	CO6	L2
9	Operators	CO6	L2
10	Operands	CO6	L3
11	Operator Types	CO6	L3
12	Examples	CO6	L3
c	**Application Areas**	**CO**	**Level**
1	Writing the program to design digital circuits in verilog.	CO1	L3
2		CO2	L4
d	**Review Questions**	-	-
1	Write the truth table of all the basic gates. Input values consisting of '0', '1', 'x', 'z'.	CO5	L2
2	What are the primitive gates supported by Verilog HDL? Write the Verilog HDL statements to instantiate all the primitive gates	CO5	L3
3	Use gate level description of Verilog HDL to design 4 to 1 multiplexer. Write truth table, top-level block, logic expression and logic diagram. Also write the stimulus block for the same.	CO5	L3
4	Explain the different types of buffers and not gates with the help of truth table, logic symbol, logic expression (bufif, buf, not, notif).	CO5	L3
5	Use gate level description of Verilog HDL to describe the 4-bit ripple carry counter. Also write a stimulus block for 4-bit ripple carry adder.	CO5	L3
6	How to model the delays of a logic gate using Verilog HDL? Give	CO5	L3

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	examples. Also explain the different delays associated with digital circuits.		
7	Write gate level description to implement function y = a.b + c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	CO5	L2
8	With syntax describe the continuous assignment statement	CO5	L3
9	Show how different delays associated with logic circuit are modeled using dataflow description.	CO6	L3
10	Explain different operators supported by Verilog HDL.	CO6	L3
11	What is an expression associated with dataflow description? What are the different types of operands in an expression?	CO6	L3
12	Discuss the precedence of operators.	CO6	L3
13	Use dataflow description style of Verilog HDL to design 4:1 multiplexer with and without using conditional operator.	CO6	L3
14	Use dataflow description style of Verilog HDL to design 4-bit adder using i. Ripple carry logic. ii. Carry look ahead logic.	CO6	L3
15	Use dataflow description style, gate level description of Verilog HDL to design 4-bit ripple carry counter. Also write the stimulus block to verify the same.	CO6	L3
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

Module – 4

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Design digital circuits using behavioral style of modeling with test bench	CO5	L2
2			
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**

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1	**Behavioral Modeling** Structured procedures	CO7	L3
2	Initial And Always	CO7	L3
3	Initial And Always	CO7	L3
4	Blocking And Non-Blocking Statements	CO7	L3
5	Blocking And Non-Blocking Statements	CO7	L3
6	Delay Control	CO7	L3
7	Generate Statement	CO7	L3
8	Event Control	CO7	L3
9	Conditional Statements	CO7	L3
10	Conditional Statements	CO7	L3
11	Multi-Way Branching	CO7	L3
12	Loops	CO7	L3
13	Loops	CO7	L3
14	Sequential And Parallel Blocks.CO7	CO7	L3
c	**Application Areas**	**CO**	**Level**
1	Design Of Digital Circuits	CO7	L3
2		CO7	L4
d	**Review Questions**	-	-
1	Describe the following statements with an example: initial and always	CO7	L3
2	What are blocking and non-blocking assignment statements? Explain with examples.	CO7	L3
3	With syntax explain conditional, branching and loop statements available in Verilog HDL behavioural description.	CO7	L3
4	Describe sequential and parallel blocks of Verilog HDL.	CO7	L3
5	Write Verilog HDL program of 4:1 mux using CASE statement.	CO7	L3
6	Write Verilog HDL program of 4:1 mux using If-else statement.	CO7	L3
7	Write Verilog HDL program of 4-bit synchronous up counter.	CO7	L3
8	Write Verilog HDL program to simulate traffic signal controller.	CO7	L3
e	**Experiences**	-	-
1		CO7	L2
2			
3			
4		CO8	L3
5			

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E2. CIA EXAM – 2

a. Model Question Paper – 2

Crs Code:	15EC53	Sem:	5	Marks:	30	Time:	75 minutes
Course:	Verilog HDL						

-	-	**Note: Answer any ONE questions from each module.**	**Marks**	**CO**	**Level**
1	a	Explain the logic gate primitives with logic symbol and truth table.	08	CO5	L2
	b	Construct a verilog model for 8:1 multiplexer	07	CO5	L3
2	a	List and explain the types of operators used in verilog. i) Arithmetic ii) Bitwise iii)Relational iv)Equality	08	CO6	L2
	b	Construct a verilog module for 4 bit Carry Look Ahead Adder (CLA).	07	CO6	L2
3	a	Explain the delay control statements used in behavioral modeling of verilog with suitable examples.	08	CO7	L2
	b	Construct a verilog description for 4:1 multiplexer using case statements in behavioral modeling of verilog.	07	CO7	L3
4	a	Explain the conditional statements with syntax and mention the examples for each type.	08	CO7	L2
	b	With example explain the structured procedures in behavioral modeling.	07	CO7	L3

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	15EC53	Sem:	5	Marks:	5	Time:	90-120 minutes
Course:	Verilog HDL						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	**USN**	**Assignment Description**	**Marks**	**CO**	**Level**
1.	1KT16EC003	Write the truth table of all the basic gates. Input values consisting of '0', '1', 'x', 'z'.	6	CO5	L2
2.	1KT16EC004	What are the primitive gates supported by Verilog HDL? Write the Verilog HDL statements to instantiate all the primitive gates	6	CO5	L3
3.	1KT16EC005	Use gate level description of Verilog HDL to design 4 to 1 multiplexer. Write truth table, top-level block, logic expression and logic diagram. Also write the stimulus block for the same.	6	CO5	L4

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4.	1KT16EC008	Explain the different types of buffers and not gates with the help of truth table, logic symbol, logic expression (bufif, buf, not, notif).	6	CO5	L3
5.	1KT16EC011	Use gate level description of Verilog HDL to describe the 4-bit ripple carry counter. Also write a stimulus block for 4-bit ripple carry adder.	6	CO5	L3
6.	1KT16EC012	How to model the delays of a logic gate using Verilog HDL? Give examples. Also explain the different delays associated with digital circuits.	8	CO5	L3
7.	1KT16EC014	Write gate level description to implement function y = a.b + c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	8	CO5	L3
8.	1KT16EC015	With syntax describe the continuous assignment statement	8	CO6	L3
9.	1KT16EC016	Show how different delays associated with logic circuit are modeled using dataflow description.	8	CO6	L3
10.	1KT16EC018	Explain different operators supported by Verilog HDL.	8	CO6	L3
11.	1KT16EC020	What is an expression associated with dataflow description? What are the different types of operands in an expression?	8	CO6	L3
12.	1KT16EC022	Discuss the precedence of operators.	8	CO6	L3
13.	1KT16EC023	Use dataflow description style of Verilog HDL to design 4:1 multiplexer with and without using conditional operator.	8	CO6	L3
14.	1KT16EC024	Use dataflow description style of Verilog HDL to design 4-bit adder using i. Ripple carry logic. ii. Carry look ahead logic.	8	CO6	L3
15.	1KT16EC025	Use dataflow description style, gate level description of Verilog HDL to design 4-bit ripple carry counter. Also write the stimulus block to verify the same.	8	CO6	L3
16.	1KT16EC026	Describe the following statements with an example: initial and always	8	CO7	L3
17.	1KT16EC027	What are blocking and non-blocking assignment statements? Explain with examples.	8	CO7	L3
18.	1KT16EC028	With syntax explain conditional, branching and loop statements available in Verilog HDL behavioural description.	7	CO7	L3
19.	1KT16EC029	Describe sequential and parallel blocks of Verilog HDL.	8	CO7	L3
20.	1KT16EC032	Write Verilog HDL program of 4:1 mux using CASE statement.	5	CO7	L3
21.	1KT16EC033	Write Verilog HDL program of 4:1 mux using If-else statement.	6	CO7	L3

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22.	1KT16EC035	Write Verilog HDL program of 4-bit synchronous up counter.	6	CO7	L3
23.	1KT16EC407	Write Verilog HDL program to simulate traffic signal controller.	8	CO7	L3
24.	1KT16EC410	Write the truth table of all the basic gates. Input values consisting of '0', '1', 'x', 'z'.	6	CO5	L2
25.	1KT16EC413	What are the primitive gates supported by Verilog HDL? Write the Verilog HDL statements to instantiate all the primitive gates	6	CO5	L3
26.	1KT16EC417	Use gate level description of Verilog HDL to design 4 to 1 multiplexer. Write truth table, top-level block, logic expression and logic diagram. Also write the stimulus block for the same.	6	CO5	L4
27.	1KT16EC425	Explain the different types of buffers and not gates with the help of truth table, logic symbol, logic expression (bufif, buf, not, notif).	6	CO5	L3
28.	1KT15EC016	Use gate level description of Verilog HDL to describe the 4-bit ripple carry counter. Also write a stimulus block for 4-bit ripple carry adder.	6	CO5	L3
29.	1KT15EC027	How to model the delays of a logic gate using Verilog HDL? Give examples. Also explain the different delays associated with digital circuits.	8	CO5	L3
30.	1KT15EC066	Write gate level description to implement function y = a.b + c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	8	CO5	L3
31.	1KT16EC041	With syntax describe the continuous assignment statement	8	CO6	L3
32.	1KT16EC042	Show how different delays associated with logic circuit are modeled using dataflow description.	8	CO6	L3
33.	1KT16EC043	Explain different operators supported by Verilog HDL.	8	CO6	L3
34.	1KT16EC044	What is an expression associated with dataflow description? What are the different types of operands in an expression?	8	CO6	L3
35.	1KT16EC045	Discuss the precedence of operators.	8	CO6	L3
36.	1KT16EC047	Use dataflow description style of Verilog HDL to design 4:1 multiplexer with and without using conditional operator.	8	CO6	L3
37.	1KT16EC048	Use dataflow description style of Verilog HDL to design 4-bit adder using i. Ripple carry logic. ii. Carry look ahead logic.	8	CO6	L3
38.	1KT16EC049	Use dataflow description style, gate level description of Verilog HDL to design 4-bit ripple carry counter. Also write	8	CO6	L3

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		the stimulus block to verify the same.			
39.	1KT16EC050	Describe the following statements with an example: initial and always	8	CO7	L3
40.	1KT16EC051	What are blocking and non-blocking assignment statements? Explain with examples.	8	CO7	L3
41.	1KT16EC052	With syntax explain conditional, branching and loop statements available in Verilog HDL behavioural description.	7	CO7	L3
42.	1KT16EC053	Describe sequential and parallel blocks of Verilog HDL.	8	CO7	L3
43.	1KT16EC057	Write Verilog HDL program of 4:1 mux using CASE statement.	5	CO7	L3
44.	1KT16EC058	Write Verilog HDL program of 4:1 mux using If-else statement.	6	CO7	L3
45.	1KT16EC059	Write Verilog HDL program of 4-bit synchronous up counter.	6	CO7	L3
46.	1KT16EC061	Write Verilog HDL program to simulate traffic signal controller.	8	CO7	L3
47.	1KT16EC063	Write the truth table of all the basic gates. Input values consisting of '0', '1', 'x', 'z'.	6	CO5	L2
48.	1KT16EC064	What are the primitive gates supported by Verilog HDL? Write the Verilog HDL statements to instantiate all the primitive gates	6	CO5	L3
49.	1KT16EC066	Use gate level description of Verilog HDL to design 4 to 1 multiplexer. Write truth table, top-level block, logic expression and logic diagram. Also write the stimulus block for the same.	6	CO5	L4
50.	1KT16EC067	Explain the different types of buffers and not gates with the help of truth table, logic symbol, logic expression (bufif, buf, not, notif).	6	CO5	L3
51.	1KT16EC068	Use gate level description of Verilog HDL to describe the 4-bit ripple carry counter. Also write a stimulus block for 4-bit ripple carry adder.	6	CO5	L3
52.	1KT16EC069	How to model the delays of a logic gate using Verilog HDL? Give examples. Also explain the different delays associated with digital circuits.	8	CO5	L3
53.	1KT16EC070	Write gate level description to implement function y = a.b + c, with 5 and 4 time units of gate delay for AND and OR gate respectively. Also write the stimulus block and simulation waveform.	8	CO5	L3
54.	1KT16EC073	With syntax describe the continuous assignment statement	8	CO6	L3
55.	1KT16EC074	Show how different delays associated with logic circuit are modeled using dataflow description.	8	CO6	L3

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56.	1KT16EC077	Explain different operators supported by Verilog HDL.	8	CO6	L3
57.	1KT16EC078	What is an expression associated with dataflow description? What are the different types of operands in an expression?	8	CO6	L3
58.	1KT17EC402	Discuss the precedence of operators.	8	CO6	L3
59.	1KT17EC403	Use dataflow description style of Verilog HDL to design 4:1 multiplexer with and without using conditional operator.	8	CO6	L3
60.	1KT17EC406	Use dataflow description style of Verilog HDL to design 4-bit adder using i. Ripple carry logic. ii. Carry look ahead logic.	8	CO6	L3
61.	1KT17EC408	Use dataflow description style, gate level description of Verilog HDL to design 4-bit ripple carry counter. Also write the stimulus block to verify the same.	8	CO6	L3
62.	1KT16EC079	Describe the following statements with an example: initial and always	8	CO7	L3
63.	1KT16EC080	What are blocking and non-blocking assignment statements? Explain with examples.	8	CO7	L3

D3. TEACHING PLAN - 3

Module - 5

Title:	Divide and Conquer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Acquiring the knowledge on basics of VHDL and difference between verilog and VHDL	CO6	L2
2	Design digital circuits using VHDL programming	CO7	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	**Introduction to VHDL** Introduction:	CO8	l2
2	Why use VHDL?, Shortcomings,	CO8	L2
3	Using VHDL for Design Synthesis,	CO8	L2
4	Design tool flow,	CO8	L2
5	Font conventions.	CO8	L2
6	**Entities and Architectures:** Introduction,	CO9	L2
7	A simple design,	CO9	L3

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8	Design entities,	CO9	L3
9	Identifiers,	CO9	L3
10	Data objects,	CO9	L3
11	Data types,	CO9	L3
12	Attributes	CO9	L3
c	**Application Areas**	**CO**	**Level**
1	Writing the program at to design digital circuits using VHDL	CO9	L3
2			
d	**Review Questions**	-	-
1	Discuss the evolution of VHDL	CO6	L2
2	List and explain the advantages and benefits of using VHDL?	CO6	L2
3	In brief discuss the shortcomings of VHDL	CO6	L2
4	Explain the digital system synthesis using VHDL in detail.	CO6	L2
5	With tool flow diagram explain design tool flow	CO6	L2
6	Explain the components of VHDL program.	CO7	L3
7	Define entity. Explain different types of ports used in VHDL entity.	CO7	L3
8	Explain different description styles supported by VHDL with example.	CO7	L3
9	Compare different description styles of VHDL with examples.	CO7	L3
10	Explain the different data objects, data types of VHDL.	CO7	L3
11	What are attributes? Explain with examples.	CO7	L3
12	Write the entity declaration 2-bit magnitude comparator.	CO7	L3
e	**Experiences**	-	-
1		CO10	L2
2			
3			
4		CO9	L3
5			

E3. CIA EXAM – 3

a. Model Question Paper – 3

Crs Code:	15EC53	Sem:	5	Marks:	30	Time:	75 minutes
Course:	Verilog HDL						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the advantages and disadvantages of VHDL.	08	CO8	L3
	b	Write a brief note on designing an entity in VHDL.	07	CO8	L3

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2	a	Define entity. Explain different types of ports used in VHDL entity.	08	CO8	L3
	b	Explain different description styles supported by VHDL with example.	07	CO9	L3
3	a	What are attributes? Explain with examples.	08	CO8	L3
	b	Write the entity declaration 2-bit magnitude comparator.	07	CO9	L3
4	a	Explain the digital system synthesis using VHDL in detail.	08	CO9	L3
	b	With tool flow diagram explain design tool flow	07	CO	L3

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	15EC53	Sem:	5	Marks:	5	Time:	90-120 minutes
Course:	Verilog HDL						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1.	1KT16EC003	Discuss the evolution of VHDL	5	CO9	L2
2.	1KT16EC004	List and explain the advantages and benefits of using VHDL?	5	CO9	L3
3.	1KT16EC005	In brief discuss the shortcomings of VHDL	5	CO9	L2
4.	1KT16EC008	Explain the digital system synthesis using VHDL in detail.	5	CO9	L3
5.	1KT16EC011	With tool flow diagram explain design tool flow	5	CO9	L2
6.	1KT16EC012	Explain the components of VHDL program.	5	CO9	L3
7.	1KT16EC014	Define entity. Explain different types of ports used in VHDL entity.	5	CO9	L2
8.	1KT16EC015	Explain different description styles supported by VHDL with example.	5	CO9	L3
9.	1KT16EC016	Compare different description styles of VHDL with examples.	5	CO9	L2
10.	1KT16EC018	Explain the different data objects, data types of VHDL.	5	CO9	L3
11.	1KT16EC020	What are attributes? Explain with examples.	5	CO9	L2
12.	1KT16EC022	Write the entity declaration 2-bit magnitude comparator.	5	CO9	L3
13.	1KT16EC023	Discuss the evolution of VHDL	5	CO9	L2
14.	1KT16EC024	List and explain the advantages and benefits of using VHDL?	5	CO9	L3
15.	1KT16EC025	In brief discuss the shortcomings of VHDL	5	CO9	L2
16.	1KT16EC026	Explain the digital system synthesis using VHDL in detail.	5	CO9	L3
17.	1KT16EC027	With tool flow diagram explain design tool flow	5	CO9	L2
18.	1KT16EC028	Explain the components of VHDL program.	5	CO9	L3

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19.	1KT16EC029	Define entity. Explain different types of ports used in VHDL entity.	5	CO9	L2
20.	1KT16EC032	Explain different description styles supported by VHDL with example.	5	CO9	L3
21.	1KT16EC033	Compare different description styles of VHDL with examples.	5	CO9	L2
22.	1KT16EC035	Explain the different data objects, data types of VHDL.	5	CO9	L3
23.	1KT16EC407	What are attributes? Explain with examples.	5	CO9	L2
24.	1KT16EC410	Write the entity declaration 2-bit magnitude comparator.	5	CO9	L3
25.	1KT16EC413	Discuss the evolution of VHDL	5	CO9	L2
26.	1KT16EC417	List and explain the advantages and benefits of using VHDL?	5	CO9	L3
27.	1KT16EC425	In brief discuss the shortcomings of VHDL	5	CO9	L2
28.	1KT15EC016	Explain the digital system synthesis using VHDL in detail.	5	CO9	L3
29.	1KT15EC027	With tool flow diagram explain design tool flow	5	CO9	L2
30.	1KT15EC066	Explain the components of VHDL program.	5	CO9	L3
31.	1KT16EC041	Define entity. Explain different types of ports used in VHDL entity.	5	CO9	L2
32.	1KT16EC042	Explain different description styles supported by VHDL with example.	5	CO9	L3
33.	1KT16EC043	Compare different description styles of VHDL with examples.	5	CO9	L2
34.	1KT16EC044	Explain the different data objects, data types of VHDL.	5	CO9	L3
35.	1KT16EC045	What are attributes? Explain with examples.	5	CO9	L2
36.	1KT16EC047	Write the entity declaration 2-bit magnitude comparator.	5	CO9	L3
37.	1KT16EC048	Discuss the evolution of VHDL	5	CO9	L2
38.	1KT16EC049	List and explain the advantages and benefits of using VHDL?	5	CO9	L3
39.	1KT16EC050	In brief discuss the shortcomings of VHDL	5	CO9	L2
40.	1KT16EC051	Explain the digital system synthesis using VHDL in detail.	5	CO9	L3
41.	1KT16EC052	With tool flow diagram explain design tool flow	5	CO9	L2
42.	1KT16EC053	Explain the components of VHDL program.	5	CO9	L3
43.	1KT16EC057	Define entity. Explain different types of ports used in VHDL entity.	5	CO9	L2
44.	1KT16EC058	Explain different description styles supported by VHDL with example.	5	CO9	L3
45.	1KT16EC059	Compare different description styles of VHDL with examples.	5	CO9	L2
46.	1KT16EC061	Explain the different data objects, data types of VHDL.	5	CO9	L3
47.	1KT16EC063	What are attributes? Explain with examples.	5	CO9	L2
48.	1KT16EC064	Write the entity declaration 2-bit magnitude comparator.	5	CO9	L3

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49.	1KT16EC066	Discuss the evolution of VHDL	5	CO9	L2
50.	1KT16EC067	List and explain the advantages and benefits of using VHDL?	5	CO9	L3
51.	1KT16EC068	In brief discuss the shortcomings of VHDL	5	CO9	L2
52.	1KT16EC069	Explain the digital system synthesis using VHDL in detail.	5	CO9	L3
53.	1KT16EC070	With tool flow diagram explain design tool flow	5	CO9	L2
54.	1KT16EC073	Explain the components of VHDL program.	5	CO9	L3
55.	1KT16EC074	Define entity. Explain different types of ports used in VHDL entity.	5	CO9	L2
56.	1KT16EC077	Explain different description styles supported by VHDL with example.	5	CO9	L3
57.	1KT16EC078	Compare different description styles of VHDL with examples.	5	CO9	L2
58.	1KT17EC402	Explain the different data objects, data types of VHDL.	5	CO9	L3
59.	1KT17EC403	What are attributes? Explain with examples.	5	CO9	L2
60.	1KT17EC406	Write the entity declaration 2-bit magnitude comparator.	5	CO9	L3
61.	1KT17EC408	Compare different description styles of VHDL with examples.	5	CO9	L2
62.	1KT16EC079	Explain the different data objects, data types of VHDL.	5	CO9	L3
63.	1KT16EC080	What are attributes? Explain with examples.	5	CO9	L2

F. EXAM PREPARATION

1. University Model Question Paper

Course:	Verilog HDL					Month / Year	Nov /2018
Crs Code:	15EC53	Sem:	5	Marks:	80	Time:	180 minutes

-	Note		Marks	CO	Level
1	a	Explain a typical design flow for designing VLSI IC circuits using the block diagram	8	CO1	L2
	b	Explain the different levels of Abstraction used for programming in Verilog.	8	CO1	L2
2	a	Explain a top-down design methodology and a bottom-up design methodology.	8	CO2	L2
	b	Explain the factors that have made Verilog HDL popular.	8	CO2	L2

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3	a	Write a note on i) Comments ii) Number Specification iii) X and Z values and iv)Identifiers and Keywords with suitable examples	8	CO3	L2
	b	Explain a Components of a Verilog Module with a neat block diagram.	8	CO3	L2
4	a	Explain $display and $monitor tasks with examples	8	CO4	L3
	b	A 4-bit parallel shift register has I/O pins as shown in the figure below. Write the module definition for this shift register. Include the list of ports and port declarations	8	CO4	L3
5	a	Explain the instantiation of gates by writing a gate level module by name gates a in Verilog.	4	CO5	L3
	b	Explain regular assignment delay in dataflow level of abstraction in Verilog.	6	CO6	L3
	c	The input output expressions for 1-bit Full Adder are given as sum= a ^ b^ c; co= (a &b)|(b&c)|(c&a). Write the gate level abstraction of 1-bit Full Adder by instantiating and, or, xor gates only.	6	CO5	L3
6	a	Write the Verilog description of 4-bit Ripple carry Adder at Gate level Abstraction	8	CO5	L3
	b	Write a program for 4-to-1 Multiplexer, Using Conditional Operators in data-flow level of abstraction in Verilog.	8	CO6	L3
7	a	Explain combined port declaration and combined ANSI C style port declaration with examples in Verilog.	4	CO7	L2
	b	Explain the conditional statements in Verilog.	6	CO7	L2
	c	Write a behavioral 4 bit counter program in Verilog.	6	CO7	L2
8	a	Explain different Loop statements in Verilog.	8	CO7	L2
	b	Write a Verilog behavioral 4 to 1 Multiplexer program using CASE statement.	8	CO7	L3
9	a	Explain the synthesis process with a block diagram.	8	CO8	L2
	b	Write the VHDL entity declaration of 4- bit Ripple Carry Adder with the help of lock diagram of 4- bit Ripple Carry adder.	8	CO9	L3
10	a	Explain the relationship between a design entity and its entity declaration and architecture body in VHDL.	8	CO9	L2
	b	Explain the declaration of constant, variable and signal in VHDL with examples.	8	CO9	L3

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2. SEE Important Questions

Course:	Design and Analysis of Algorithms					Month / Year	DEC /2018	
Crs Code:	15EC53	Sem:	5	Marks:	80	Time:	180 minutes	
	Note	Answer all FIVE full questions. All questions carry equal marks.				-	-	
Module	Qno.	Important Question				**Marks**	**CO**	**Year**
1	1	Explain a typical design flow for designing VLSI IC circuit using block diagram.				06	CO1	2017
	2	Explain the top down design methodology and bottom up design methodology				10	CO2	2017
2	1	With a block diagram of 4 bit Ripple carry counter explain the design heirarachy				10	CO2	2017
	2	Explain the trends in Hardware Description Languages(HDL).				6	CO1	2017
3	1	With a neat block diagram explain the components of verilog module.				6	CO3	217
	2	Explain the following data types with an example verilog I) nets ii) registers iii) integers iv) real v) time registers				10	CO4	2017
4	1	Explain the port connection rules				6	CO3	217
	2	Explain the two methods of connecting ports to external signals with an example				10	CO4	2017
5	1	What are rise, fall and turn off delays? How they are specified in verilog.				6	CO5	2017
	2	Design 2 to1 multiplexer using bufif0 and bufif1 gates. They delay specifications for these gates are as follows: write the gate level description and stimulus.				10	CO5	2017
		Delay	Min	Typ	max			
		Rise	1	2	3			
		Fall	3	4	5			
		Turn-off	5	6	7			

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6	1	Write a verilog data flow level of abstraction for 4 to 1 multiplexer using conditional operator.	6	CO6	2017
	2	Write a verilog data flow description for 4 bit full adder with carry lookahead	10	CO6	2017
7	1	Explain the blocking assignment statements and non blocking assignment statements with relevant examples	8	CO7	2017
	2	Write a note on following loops statements I) while loop ii) forever loop	8	CO7	2017
8	1	Explain the sequential and parallel blocks with examples	8	CO7	2017
	2	Write a verilog program for 8 to 1 multiplexer using case statements	8	CO7	2017
9	1	Explain the synthesis process with block diagram	8	CO8	2017
	2	Write a VHDL program for 2 bit comparator using data-flow description	8	CO9	2017
10	1	Explain the declaration of constant, variable and signal in VHDL with example.	8	CO8	2017
	2	Write a VHDL program for Half adder using Behavioral description	8	CO9	2017